Reply Under 37 CFR 1.116
Expedited Procedure
Technology Center 2634

This listing of claims will replace all prior versions, and listings, of the claims in this application:

Listing of Claims

Subj

Claim 1 (original): A cascaded integrator comb digital filter, comprising:

a cascaded integrator structure;

a cascaded comb structure;

a first rate change component, located between said cascaded integrator structure and said cascaded comb structure; and

a second rate change component, located with said cascaded comb structure.

Claim 2 (original): The cascaded integrator comb digital filter according to Claim 1, wherein said first rate change component subsamples output received from said cascaded integrator structure and outputs a reduced rate signal to said cascaded comb structure.

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Claim 3 (original): The cascaded integrator comb digital filter according to Claim 1, wherein said cascaded integrator structure comprises a plurality of integrator stages.

Claim 4 (original): The cascaded integrator comb digital filter according to Claim 1, further comprising a third rate change component.

Claim 5 (original): The cascaded integrator comb digital filter according to Claim 1, further comprising a plurality of additional rate change components.

Claim 6 (original): The cascaded integrator comb digital filter according to Claim 1, further comprising a signal generating component providing an oversampled signal as input to said cascaded integrator structure.

Claim 7 (original): The cascaded integrator comb digital filter according to Claim 6, wherein said signal generating component comprises a delta-sigma modulator.

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Claim 8 (original): The cascaded integrator comb digital filter according to Claim 1, wherein said cascaded integrator structure comprises a plurality of integrator stages and wherein said cascaded comb structure comprises a plurality of comb stages, said plurality of integrator stages and said plurality of comb stages having an equivalent number of stages.

Claim 9 (original): The cascaded integrator comb digital filter according to Claim 8, wherein at least two comb stages of said plurality of comb stages have different delay values.

Claim 10 (original) The cascaded integrator comb digital filter according to Claim 1, further comprising a resonator component, and wherein said cascaded comb structure comprises a plurality of comb stages.

Claim 11 (original): The cascaded integrator comb digital filter according to Claim 10, wherein said resonator component is located between two comb stages of said plurality of comb stages.

Claim 12 (original): The cascaded integrator comb digital filter according to Claim 10, further comprising a plurality of resonators located among said plurality of comb stages.

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Claim 13 (currently amended): A pre-decimated integrator filter section, comprising:

a data rate change component; and

a first integrator structure comprising at least one recursive integrator stage, said first integrator structure receiving data at a rate established by said data rate change component, said first integrator structure modifying data received from said data rate change component;

wherein the pre-decimated integrator filter section outputs data equivalent to data that would be output by a post-decimated integrator filter section having an equal number of integrator stages.

Claim 14 (original): The pre-decimated integrator filter section according to Claim 13, further comprising a second integrator structure having one or more integrator stages.

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Claim 15 (currently amended): The pre-decimated integrator filter section according to Claim 13, wherein said first integrator structure comprises a[[n]] recursive integrator stage and a plurality of multipliers.

Claim 16 (original): The pre-decimated integrator filter section according to Claim 13, wherein said data rate change component comprises a serial to parallel converter.

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Claim 17 (original): The pre-decimated integrator filter section according to Claim 13, further comprising a read only memory device, said read only memory device being used by said first integrator structure to modify data received from said data rate change component.

Claim 18 (original): The pre-decimated integrator filter section according to Claim 13, wherein said first integrator structure modifies data received from said data rate change component by applying coefficients stored in a look-up table.

Claim 19 (currently amended): The pre-decimated integrator filter section according to Claim 13, wherein said first integrator structure comprises a plurality of reduced rate parallel signal paths with a[[n]] recursive integrator stage and a plurality of coefficient multipliers for each path.

Claim 20 (currently amended): A method of performing a pre-decimated cascaded integration in a filter section, comprising the steps of:

changing the data rate of data being received by an integrator structure;

performing a first integration procedure on data received at the changed data rate, wherein the first integration procedure includes at least one recursive integrator stage;

executing a second integration procedure on data output by said first integration procedure, wherein the second integration procedure includes at least one additional recursive integrator stage; and

outputting data equivalent to data that would be output by a post-decimated cascaded integrator having an equal number of integrator stages.

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Claim 21 (currently amended): A method according to Claim 20, wherein said executing step comprises processing received data with a plurality of parallel recursive integrator stages.

Claim 22 (original): A method according to Claim 20, wherein said changing step comprises converting a received serial data stream to a parallel signal having a plurality of parallel paths and decimating the received data by a factor equal to the number of parallel paths.

Claim 23 (original): The method according to Claim 20, wherein said performing step further comprises modifying the received data by multiplication by determined coefficients.

Claim 24 (original): The method according to Claim 20, wherein said performing step comprises a step of accessing a memory device, data held by said memory device being used during said performing step to modify data received from said data rate change component.

Claim 25 (original): The method according to Claim 20, wherein said performing step includes a combining procedure further modifying data received at the changed data rate.

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Claim 26 (original): A tailored response cascaded integrator comb digital filter, comprising:

cascaded integrator means;

cascaded comb means;

first rate change means, located between said cascaded integrator means and said cascaded comb means; and

second rate change means, located with said cascaded comb means.

Claim 27 (original): The tailored response cascaded integrator comb digital filter according to Claim 26, further comprising a resonator means.

Claim 28 (original): The tailored response cascaded integrator comb digital filter according to Claim 27, wherein said resonator means is located with said cascaded comb means.

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Claim 29 (original): The tailored response cascaded integrator comb digital filter according to Claim 26, wherein said cascaded comb means comprises a plurality of comb stages.

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Claim 30 (original): The tailored response cascaded integrator comb digital filter according to Claim 29, wherein at least two comb stages of said plurality of comb stages have different delay values.